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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/725,855
Filing Date: December 02, 2003
Appellant(s): PLINE ET AL.

Steven E. Dicke
Reg. No. 38,431
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/24/2007 appealing from the Office action mailed 11/02/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,119,245	HIRATSUKA	9-2000
5428630	WENG	5-1995
2003/0028733	TSUNODA	2-2003

20030115518	KLEVELAND	5-2003
5,809,090	BUTERNOWSKY	9-1998

Riley, Martyn. Reed-solomon codes, Aug 2, 2002,

http://www.4i2i.com/reed_solomon_codes.htm, Pages 1-2

(9) Grounds of Rejection

Claims 1-8,10,11,13-17,23 and 26-35 are rejected under 35 U.S.C. 102(b) as being unpatentable by Hiratsuka (6,119,245).

As to claim 1, Hiratsuka discloses a data storage and retrieval system operating on a host computer, the data storage and retrieval system comprising:

a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device, the sparing system comprising computer readable instructions stored in the host memory of the host computer (column 2, lines 31-41); and

an error correction code system configured to encode data with an error correction code, store the data into the memory device, and decode the encoded data with the error correction code to retrieve the data from the memory device, the error correction code system comprising computer readable instructions stored in the host memory of the host computer (column 5, lines 46-53).

As to claim 2, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the host memory (column 5, lines 54-57).

As to claim 3, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table stored in the memory device (Figure 15, column 7, lines 34-37).

As to claim 4, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from a tester that tests the memory device (column 7, lines 16-67).

As to claim 5, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table comprising entries obtained from the sparing system that is configured to test the memory device to obtain the entries for the sparing table (column 7, lines 16-67).

As to claim 6, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table, and the sparing system and the error correction code system are configured to update the sparing table as defective memory sections are detected in the memory device (column 7, lines 46-53).

As to claim 7, Hiratsuka discloses the data storage and retrieval system of claim 1, where the sparing system comprises a sparing table and the error correction code system is configured to detect defective memory sections in the memory device, and the sparing system is configured to update the sparing table with address locations of the detected defective memory sections in the memory device (column 5, lines 54-57 & column 7, lines 46-53).

As to claim 8, Hiratsuka discloses the data storage and retrieval system of claim 7, where the error correction code system is configured to correct errors in a selected

memory section of the memory device, count the errors to obtain an error count and compare the error count to a threshold value to establish if the selected memory section is defective (column 7, lines 38-67).

As to claim 10, Hiratsuka discloses the data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode all data stored in the memory device (column 5, lines 46-53).

As to claim 12, Hiratsuka discloses the data storage and retrieval system of claim 1, where the error correction code system is configured to encode and decode selected data stored in the memory device (column 5, lines 46-53).

As to claim 13, Hiratsuka discloses a host computer, comprising:

a host host memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device (column 7, lines 38-53); and

a host processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (column 7, lines 54-67).

As to claim 14, Hiratsuka discloses the host computer of claim 13, where the host processor executes instructions to replace addresses before the processor executes instructions to encode and decode data with the error correction code during data transfers (column 7, lines 16-30).

As to claim 15, Hiratsuka discloses the host computer of claim 13, where the host processor executes instructions to encode data with the error correction code before the processor executes instructions to replace addresses during a write operation (column 1, lines 51-61).

As to claim 16, Hiratsuka discloses the host computer of claim 13, where the processor executes instructions to provide sequential address data transfers between the storage device and the host computer (column 2, lines 31-41).

As to claim 17, Hiratsuka discloses the host computer of claim 16, where the sequential address data transfers are divided into sub-transfers around addresses of defective memory sections that are replaced with addresses of spare memory sections (column 2, lines 31-41).

As to claim 23, Hiratsuka discloses a computer system, comprising:

means for correcting errors in data retrieved from a storage style memory device, the means for correcting errors comprising computer readable instructions stored in a host memory of a host computer system (column 5, lines 46-53);

means for identifying defective sections of memory in the storage style memory device, where the defective sections of memory provide more errors than a predetermined threshold value (column 7, lines 54-67); and

means for sparing the defective sections of memory with replacement sections of memory in the storage style memory device, the means for sparing comprising computer readable instructions stored in the host memory of the host computer system (column 7, lines 63-66).

As to claim 26, Hiratsuka discloses the computer system of claim 23, where the means for identifying comprises:

means for counting the number of errors in a selected section of memory in the storage style device (columns 7-8, lines 67-3);

means for comparing the number of errors to the predetermined threshold value to obtain a compare result (column 8, lines 3-8); and

means for indicating if the selected section of memory is defective based on the compare result (column 8, lines 8-11).

As to claim 27, Hiratsuka discloses the computer system of claim 23, where the means for identifying comprises:

means for storing an address location of one of the defective sections (column 14, lines (column 8, lines 8-11); and

means for storing an address location of one of the replacement sections, where the address location of one of the replacement sections corresponds to the address location of one of the defective sections (column 7, lines 10-15).

As to claim 28, Hiratsuka discloses the computer system of claim 27, where the means for sparing comprises means for replacing the address location of one of the defective sections with the corresponding address location of one of the replacement sections during data transfers between the computer system and the storage style memory device (column 7, lines 31-37).

As to claim 29, Hiratsuka discloses a method for storing and retrieving data, comprising:

providing a host computer and a memory device (column 5, lines 31-34);

providing computer-executable sparing instructions and error correction code instructions (column 6, lines 40-43);

replacing addresses for defective memory sections in a memory device with addresses for replacement memory sections in the memory device by executing the sparing instructions on the host computer (column 2, lines 31-41);

providing the addresses for the replacement memory sections to the memory device during read and write operations with the memory device by executing the error correction code instructions on the host computer (column 7, lines 31-37;

encoding original data with an error correction code to write encoded data into the memory device by executing the error correction code instructions on the host computer (column 5, lines 46-48); and

decoding data retrieved from a selected memory section of the memory device with the error correction code by executing the error correction code instructions on the host computer (column 5, lines 49-53).

As to claim 30, Hiratsuka discloses the method of claim 29, comprising:

maintaining a table of the addresses for defective memory sections and the addresses for replacement memory sections (column 5, lines 54-57 & column 7, lines 34-37); and

searching the table to match original addresses with the addresses for defective memory sections (column 7, lines 23-37).

As to claim 31, Hiratsuka discloses the method of claim 29, comprising:

updating a table with new addresses for defective memory sections (column7, lines 11-15); and

assigning new addresses for replacement memory sections that correspond with the new addresses for defective memory sections (column 7,lines 16-30).

As to claim 32, Hiratsuka discloses the method of claim 29, comprising:

counting errors in the data retrieved from the selected memory section to obtain an error count (columns 7-8, lines 67-3);

comparing the error count to error correction capabilities of the error correction code (column 8, lines 3-8); and

indicating the selected memory section is defective if the number of errors exceeds a predetermined portion of the error correction capabilities (column 8, lines 8-11).

As to claim 33, Hiratsuka discloses a method for storing and retrieving data, comprising:

providing a host computer and a storage style memory device (Figure 1.110 & column 6, lines 16-18);

providing computer-executable sparing instructions and error correction code instructions (column 7, lines 38-45);

sparing out sections of memory in the storage style memory device by executing the sparing instructions on the host computer (column 7, lines 54-67); and

encoding and decoding data stored in the storage style memory device with an error correction code by executing the error correction code instructions on the host computer (column 5, lines 46-53).

As to claim 34, Hiratsuka discloses the method of claim 33, comprising:

detecting grown defective sections of memory in the storage style memory device (column 7, lines 54-63); and

sparing out the detected grown defective sections of memory (column 7, lines 63-67).

As to claim 35, Hiratsuka discloses the method of claim 33, comprising:

encoding only selected data (column 5, lines 46-48); and

decoding only the encoded data stored in the storage style memory device (column 5, lines 49-53).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Martyn Riley (Non patent literature).

Hiratsuka discloses a data storage retrieval system operating on a host computer that provides a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device (see claim rejection 1). Error correction code is used to encode and decode that data while the system stores and retrieves that data from the memory (see claim rejection 1). Hiratsuka fails to disclose wherein the error correction code is a Reed-Solomon error correction code.

Martyn Riley discloses an introduction to error correction codes with a wide range of applications in digital communications and storage (Page 1, lines 4-5). Martyn Riley does disclose wherein the error correction code is a Reed-Solomon error correction code (Page 1, lines 4-5)

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's error correction code with Martyn Riley's Reed-Solomon error correction code. A person of ordinary skill in the art would have been motivated to make the modification because Reed-Solomon codes can provide recovery for data that has encounter an error during transmission or while being stored (Martyn Riley: Page 1, lines 5-15).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Weng (5,428,630).

As to claim 9, Hiratsuka the data storage and retrieval system of claim 7, where the error correction code system is configured to correct errors in a selected memory section of the memory device, count the errors to obtain an error count and compare the error count to a threshold value to establish if the selected memory section is defective (see claim rejection 8). Hiratsuka fails to disclose wherein the threshold value is greater than 50% of a power of the error correction code.

Weng discloses a method and system for verifying the integrity of data written to a memory (Abstract, lines 1-2). The data is encoded and stored with error correction symbols in the memory and errors are detected when the decoder generates an error signal when the number of errors is greater than predetermined threshold number

(Abstract, lines 8-19). Weng does disclose wherein the threshold value is greater than 50% of a power of the error correction code (column 8, lines 49-56 & column 9, lines 10-20)

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's threshold value with Weng's threshold value greater that 50% of a power of the correction code. A person of ordinary skill in the art would have been motivated to make the modification because a greater threshold allows for more data to be corrected and inturn less data is lost (Weng: column 9,lines 12-20).

Claims 18,19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Tsunoda (2003/0028733).

As to claim 18, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the host memory stores instructions for a digital camera and the processor executes the instructions to perform functions of the digital camera.

Tsunoda discloses an ECC control circuit in the memory interface control unit that checks whether an errors is present or not in data read from the memory, and corrects the data if an error is present. Tsunoda also discloses if a sector as a target for reading is a failed sector, an alternative sector control circuit detects an alternative sector as a target for reading, and data is read from the detected alternative sector (Page 7, ¶ 0097, lines 11-18). Tsunoda does disclose wherein the memory stores instructions for a digital camera and the host processor executes the instructions to perform functions of the digital camera (Page 6, ¶ 0096, lines 16-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's memory storing instructions with Tsunoda's memory that stores instructions for a digital camera. A person of ordinary skill in the art would have been motivated to make the modification because if a sector in the memory is bad the alternative sector control circuit will provide a alternative sector to read or write data to (Tsunoda: Page 7, ¶ 0097, lines 24-28)

As to claim 19, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers

between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the memory stores instructions for a personal digital assistant and the host processor executes the instructions to perform functions of the personal digital assistant.

Tsunoda discloses an ECC control circuit in the memory interface control unit that checks whether an errors is present or not in data read from the memory, and corrects the data if an error is present. Tsunoda also discloses if a sector as a target for reading is a failed sector, an alternative sector control circuit detects an alternative sector as a target for reading, and data is read from the detected alternative sector (Page 7, ¶ 0097, lines 11-18). Tsunoda does disclose wherein the memory stores instructions for a personal digital assistant and the host processor executes the instructions to perform functions of the personal digital assistant. (Page 6, ¶ 0096, lines 16-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's memory storing instructions with Tsunoda's memory that stores instructions for a personal digital assistant. A person of ordinary skill in the art would have been motivated to make the modification because if a sector in the memory is bad the alternative sector control circuit will provide a alternative sector to read or write data to (Tsunoda: Page 7, ¶ 0097, lines 24-28)

As to claim 20, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a

processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the storage device comprises a magnetic random access memory.

Tsunoda discloses an ECC control circuit in the memory interface control unit that checks whether an errors is present or not in data read from the memory, and corrects the data if an error is present. Tsunoda also discloses if a sector as a target for reading is a failed sector, an alternative sector control circuit detects an alternative sector as a target for reading, and data is read from the detected alternative sector (Page 7, ¶ 0097, lines 11-18). Tsunoda does disclose wherein the storage device comprises a magnetic random access memory (Page 10, ¶ 0124, lines 9-12).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Tsunoda's MRAM in place of Hiratsuka's flash memory. A person of ordinary skill in the art would have been motivated to make the modification because MRAM is also non-volatile, meaning it can be used to replace Flash and unlike Flash, MRAM does not degrade during writing, nor is it slower to write than to read.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Kleveland (2003/0115518).

As to claim 21, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the storage device comprises a phase change random access memory.

Kleveland discloses a memory device and method for redundancy and self repair (Abstract, lines 1-2). Kleveland does disclose wherein the storage device comprises a phase change random access memory (Page 7, ¶ 0053, lines 14-18).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Kleveland's phase change random access memory in place of Hiratsuka's flash memory. A person of ordinary skill in the art would have been motivated to make the modification because phase change random access memories are a well-known alternative (Kleveland: Page 7, ¶ 0053, lines 14-18).

As to claim 22, Hiratsuka discloses a host computer, comprising: memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a processor that executes the instructions to encode and decode data stored in the

storage device with the error correction code and to replace addresses of defective memory sections with addresses of spare memory sections, where the addresses of the spare memory sections are provided to the storage device during data transfers between the storage device and the host computer (see claim 13 rejection). Hiratsuka fails to disclose wherein the storage device comprises a probe-based memory.

Kleveland discloses a memory device and method for redundancy and self repair (Abstract, lines 1-2). Kleveland does disclose wherein the storage device comprises a probe-based memory (Page 7, ¶ 0053, lines 14-18).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Kleveland's probe-based memory in place of Hiratsuka's flash memory. A person of ordinary skill in the art would have been motivated to make the modification because probe-based memories are a well-known alternative (Kleveland: Page 7, ¶ 0053, lines 14-18).

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiratsuka taken in view of Buternowsky (5,809,090).

As to claim 24, Hiratsuka discloses a data storage retrieval system that provides a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device when the defective sections of the memory provide more errors than a predetermined threshold value (see claim rejection 23). Hiratsuka also discloses correcting errors in data retrieved from the memory device. Hiratsuka fails to disclose wherein the means for correcting errors comprises a multiple-bit per symbol error correction code.

Buternowsky discloses a communication system wherein response signals are in the form of digital packets, including forward error correction encoding and digital symbols that each consists of predetermined number of bits (Abstract, lines 3-5). Buternowsky does disclose wherein the means for correcting errors comprises a multiple-bit per symbol error correction code (column 6, lines 23-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's error correction code with Buternowsky's multiple-bit per symbol ECCI. A person of ordinary skill in the art would have been motivated to make the modification because three bit symbols allow eight distinct symbols (Buternowsky: Page 6, lines 24-25).

As to claim 25, Hiratsuka discloses a data storage retrieval system that provides a sparing system configured to replace defective memory sections of a memory device with replacement memory sections of the memory device when the defective sections of the memory provide more errors than a predetermined threshold value (see claim rejection 23). Hiratsuka also discloses correcting errors in data retrieved from the memory device. Hiratsuka fails to disclose wherein the means for correcting errors comprises a single-bit per symbol error correction code.

Buternowsky discloses a communication system wherein response signals are in the form of digital packets, including forward error correction encoding and digital symbols that each consists of predetermined number of bits (Abstract, lines 3-5). Buternowsky does disclose wherein the means for correcting errors comprises a single-bit per symbol error correction code (column 6, lines 23-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Hiratsuka's error correction code with Buternowsky's single-bit per symbol ECC scheme. A person of ordinary skill in the art would have been motivated to make the modification because having a single-bit symbol would reduce the amount of noise during transmission of the error correction code (Buternowsky: Page 6, lines 24-25).

(10) Response to Argument

On page 8 of the Appeal Brief, applicant argues limitations of claim 1 shown below:

> *Hiratsuka discloses a disk controller including hardware components that provide ECC encoding and decoding, data error information management, and address conversion. The disk controller includes a host interface 121 for communicating with a host computer. The host computer in Hiratsuka does not perform any of the error correction, data error information management, or address conversion functions. The host computer in Hiratsuka provides command information and address information to semiconductor device 100 through host interface 121. (Col. 6, lines 40-43). Determination of whether or not address conversion is to be performed and rewriting of logical memory numbers are performed by micro CPU 131. (Col. 6, lines 21-24). Micro CPU 131 uses conversion table 128, which is part of disk controller section 120, to perform address conversion. (See col. 6, lines 51-60). ECC control section 126, which is part of disk controller section 120, compiles the ECC data. (See col. 6, lines 63-67). Both the address conversion and ECC functions disclosed by Hiratsuka are performed independently from the host computer and without the host computer's knowledge. The host computer just reads and writes data to the memory device 100 without being involved in the address conversion or ECC functions.*
>
> *In contrast, claim 1 recites a system that operates on a host computer. In addition, the sparing system and the error correction code system comprise computer readable instructions stored in a host memory of the host computer. The sparing system and the error correction code system recited by claim 1 are implemented using computer readable instructions executed on the host computer. The host computer performs the sparing and ECC functions. The memory device recited by claim 1 has no knowledge or control of the sparing*

system or the ECC system. In contrast, Hiratsuka discloses address conversion and ECC functions that are performed by the storage device without knowledge or control by the host computer.

The examiner respectfully disagrees. As stated in the final rejection the disk device section (Figure 1.100) is part of the "host system" as applicants "host memory" shown in figure 1.28 is considered part of "host system". Hiratsuka discloses a semiconductor storage device that is directly interfaced with a host (Figure 1, column 5, lines 20-23). The semiconductor storage device is part of your host computer the same way a hard drive is part of your desktop computer. Hiratsuka does not disclose the semiconductor storage device being accessed over a network, nor does Hiratsuka disclose the semiconductor storage device being accessed by multiple computers. Since program memory 132 stores the computer readable instructions for performing the functions of the sparing system and the error correction code system and the memory 132 is located on the "host system" the host does in fact have knowledge and control of the functions being performed (column 6, lines 30-36).

On pages 9-11 of the Appeal Brief, applicant argues limitations of independent claims 13,23,29 and 33 with the same reasoning used in the argument of claim 1. Examiner respectfully disagrees for the same reasons previously discussed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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